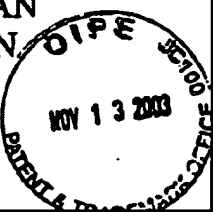


INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 57454-963		SERIAL NO. Divisional of Serial No. 09/903,735 10/633576	
							
APPLICANT Hiroshi MAEDA, ET AL.							
FILING DATE August 5, 2003				GROUP To be assigned			
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
TT	6,424,011	07/2002	Assaderaghi et al	257	350	/	
TT	6,255,151	07/2001	Fukuda et al	257	296		
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
TT	M. Igarashi, A. Harada, H. Amishiro, H. Kawashima, N. Morimoto, Y. Kusumi, T. Saito, A. Ohsaki, T. Mori, T. Fukada, Y. Toyoda, K. Higashitani, and H. Arima, "The Best Combination Of Aluminum and Copper Interconnects For a High Performance 0.18µm CMOS Logic Device," IEDM98, 1998, PP. 829-832.						
TT	J. Heidenreich, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, T. McDevitt, A. Stamper, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, S. Luce, and J. Slattery, "Copper Dual <u>Damascene</u> Wiring for Sub-0.25µm CMOS Technology," PP. 13-15.						
EXAMINER <i>Thun KMC</i>				DATE CONSIDERED 09/03/04			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.